#26/Affidavit 2/15/01 V.Vadnais

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application: No. 09/160,657 Group Art Unit 2822

Filed: September 25, 1998 Attorney Docket: UIL-1001

Inventor(s): Joseph W. Lyding et al. Examiner: M. Guerrero

For: SEMICONDUCTIVE DEVICES AND METHODS FOR SAME

Assistant Commissioner of Patents
Washington, D.C. 20231

CERTIFICATION UNDER RULE 37 CFR 1.10
I hereby certify that this document and the documents referred to as enclosed therein are being deposited with the United States Postal Service on the date indicated below, in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EK741950485US addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231.

Judy Betts 2-8-01
Judy Betts Date

AFFIDAVIT OF JOSEPH W. LYDING

State of Illinois)
)
County of Champaign)

Joseph W. Lyding, being duly sworn, deposes and states:

1. I am a joint inventor of subject matter disclosed and claimed in application 09/160,657.
2. I have received a Bachelor of Science degree from Northwestern University in 1976, a Masters of Science degree from Northwestern University in 1978, and a Doctor of Philosophy degree from Northwestern University in 1983. I am a Professor of Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign and have been since August 1993.
3. I have read and understood the specification of application 09/160,657 and am conversant with the field of semiconductor devices and semiconductor device processing, particularly in relation to field effect transistor devices including MOS devices and processing. I have coauthored a number of published papers in professional journals concerning the subject matter of this application, including J. W. Lyding, K. Hess, and I. C. Kizilyalli, "Reduction of hot electron degradation in metal oxide semiconductor transistors by deuterium processing, *Applied Physics Letters*, **68** (18), pp. 2526-2528, 29 April 1996, ("Applied Physics Letters") and I. C. Kizilyalli, J. W. Lyding, and K.

Hess, "Deuterium Post-Metal Annealing of MOSFET's for Improved Hot Carrier Reliability," *IEEE Electron Device Letters*, Vol. 18, No. 3, pages 81-83, March 1997 ("IEEE Electron Device Letters"). Copies of these publications are attached hereto as Exhibits A and B respectively.

4. I have read and understood the specification and claims of US Patent 6023093.

5. The specification of application 09/160,657 discloses annealing of MOS transistor structures in deuterium, including annealing subsequent to fabrication of the gate, source and drain contacts to dispose deuterium at the interface of the (silicon) substrate and the gate insulator (page 11, line 16-page 12, line 4 and Fig. 1). In particular, annealing in a gas ambient comprising 10% deuterium and 90% nitrogen for 60 minutes at 400 °C is disclosed, including description at page 21, line 18 to page 22, line 2. This annealing process is effective to significantly reduce effects associated with depassivation of the device by hot-carrier (e.g. hot electron) effects. This improvement is illustrated by dramatic decreases in the degradation of threshold voltage and transconductance as compared to hydrogen passivation – see page 17, line 18 to page 18, line 2 and page 21, line 18 to page 23, line 3 and Figs. 2 and 3. Applied Physics Letters discloses the same deuterium processing parameters and substantially reduced susceptibility to hot electron degradation effects, for example note FIG. 1 (sintering in a 90% nitrogen, 10% deuterium ambient at 400 °C for 1 hour, i.e. the same parameters as disclosed in application 09/160,657) and FIG. 2, showing the same results as Fig. 2 and Fig. 3 of application 09/160,657.

6. In a publication by Thomas G. Ference, Jay S. Burnham, William F. Clark, Terence B. Hook, Steven W. Mittl, Kimbal M. Watson, and Liang-Kai Keven Han "The Combined Effects of Deuterium Anneals and Deuterated Barrier-Nitride Processing on Hot-Electron Degradation in MOSFET's", *IEEE Transactions on Electron Devices*, vol. 46, No. 4, pp. 747-753, April 1999, ("IEEE Electron Devices") there is described annealing of various MOS transistor device structures in deuterium to passivate the device to make it more robust to hot-electron damage. Although the publication is primarily directed to experiments carried out on a MOS device incorporating a silicon nitride barrier layer around the gate, as depicted in Fig. 1, there is also described annealing of such a MOS transistor structure without the barrier nitride layer shown in Fig. 1. The annealing is carried out in a gas ambient comprising 10% deuterium and 90% nitrogen for 60 minutes at 400 °C and Fig. 4B illustrates the results of such annealing at First Metal of a MOS transistor without the barrier nitride layer shown in Fig. 1. Fig. 4B indicates that a deuterium concentration greater than 10^{16} cm^{-3} at the gate oxide/silicon interface and in the gate oxide layer is obtained under these conditions. A copy of this publication is attached hereto as Exhibit C.

7. Consequently, the deuterium annealing process disclosed in application 09/160,657, referred to in paragraph 5 above, is substantially the same as the deuterium annealing process described in the IEEE Electron Devices

publication with reference to Fig. 4B (First Metal anneal without the silicon nitride barrier depicted in Fig. 1). Thus, the deuterium annealing process under conditions outlined in paragraph 5 above and as described in application 09/160,657, would result in a concentration of at least about 10^{16} cm^{-3} deuterium at the gate oxide (dielectric film)/silicon (substrate) interface and in the gate oxide (dielectric film) of the transistor device. Claim 1 of US Patent 6023093 recites a concentration of at least about 10^{16} cm^{-3} deuterium being present in a film (exemplified in claim 2 as a dielectric film) adjacent to a transistor gate.

Also, as noted above in paragraph 5, the disclosure in application 09/160,657 of the effect of the disclosed deuterium annealing process is to reduce and better resist aging due to hot carrier effects, i.e., as claimed in claim 1 of US Patent 6023093, to substantially reduce degradation associated with hot carrier effects.

Joseph W. Lyding

Joseph W. Lyding

Sworn to and subscribed before me this
6 Day of February, 2001

Madge L. Nornholm

Notary Public

"OFFICIAL SEAL"
MADGE L. NORNHOLM
Notary Public, State of Illinois
My Commission Expires 03/24/04

Reduction of hot electron degradation in metal oxide semiconductor transistors by deuterium processing

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We report experimental results that replacing hydrogen with deuterium during the final wafer sintering process greatly reduces hot electron degradation effects in metal oxide semiconductor transistors due to a new giant isotope effect. Transistor lifetime improvements by factors of 10–50 are observed. A plausible physical theory suggests that the benefits of deuterium use may be general and also applicable to other areas of semiconductor device processing and fabrication. © *1996 American Institute of Physics.* [S0003-6951(96)00418-4]

The time-dependent degradation of metal oxide semiconductor (MOS) transistor performance resulting from hot (energetic) electron effects has been an area of considerable study over the past 25 years.[1] According to established theory, this aging process is thought to occur in part as the result of hot electrons stimulating the desorption of hydrogen from the Si/SiO_2 interface region. Hydrogen is introduced by necessity during several device processing steps as, for example, during the sintering of the wafers at elevated temperature in a hydrogen ambient.[2] While this process improves device function, it sets the stage for subsequent hot electron degradation. In this letter we demonstrate an alternative process in which the interface states are passivated by deuterium instead of hydrogen. Transistors that have been annealed with deuterium show a greatly reduced degradation due to hot electron effects.

The idea of using deuterium instead of hydrogen was in part inspired by experiments in which a scanning tunneling microscope (STM) was used to stimulate the desorption of hydrogen from Si(100)2×1:H surfaces under ultrahigh vacuum (UHV) conditions.[3] Following the suggestion of Avouris,[4] these experiments were extended to deuterated surfaces in order to explore more fully the surface science issues of this process. From these new experiments it was discovered that deuterium is much more difficult to remove under the conditions used to desorb hydrogen.[5] While there are clearly many differences between a free surface in UHV and a buried Si/SiO_2 interface, this result suggests the possibility for a sizable isotope effect if hydrogen is replaced by deuterium during the conventional wafer sintering step. To test for the advantages of using deuterium, uncapped complementary metal oxide semiconductor (CMOS) wafers fabricated at Bell Laboratories were subjected to the deuterium sintering process at Illinois and then returned to Bell Laboratories for electrical stress testing.

The wafers used for our tests contained *n*-channel metal oxide semiconductor (NMOS) transistor structures fabricated using the Bell Laboratories 0.5 μm 3.3 V CMOS technology.[6] However, the following three changes were made: (i) the gate oxide was reduced to $t_{ox} \sim 55$ Å, (ii) the doping in the *p*-well was increased, and (iii) the phosphorus doped lightly doped drain region was replaced by a shallow arsenic implanted (dose = 4×10^{14} cm^{-2} and energy = 30 keV) source-drain extension region. These process modifications enhance the peak value for the source-drain electric field near the drain edge of the gate, resulting in more channel hot electrons. The shallow source-drain extension ensures that these hot electrons are near the Si/SiO_2 interface, where they will cause significant interface damage. The interface damage, caused by these hot carriers, can easily be observed by monitoring the change in the NMOS transistor transconductance (i.e., $g_m = \Delta I_{DS}/\Delta V_{GS}|_{V_{DS}=0.1\ \mathrm{V}}$) or by the shift in the transistor threshold voltage V_{TH}.[7]

For this study, accelerated hot carrier dc stress experiments were performed on transistors with varying gate lengths (0.5–15 μm) at peak substrate current conditions. The applied (accelerated) stress source drain voltage was $V_{DS}=5$ V and the source gate voltage was $V_{GS}=2$ V. Stress experiments performed at lower voltages ($V_{DS}=3.8$ V and $V_{GS}=1.5$ V) and shorter gate lengths (0.3 and 0.4 μm) give results similar to the ones reported below. Prestress transistor measurements demonstrate that devices sintered in hydrogen or deuterium have identical electrical characteristics (e.g., transconductance, subthreshold slope, threshold voltage, saturation current, substrate current, etc.).

Figure 1 shows the g_m degradation as a function of stress time for NMOS transistors with five gate lengths ranging from 0.5 to 0.7 μm. Figure 2 shows the threshold voltage increase as a function of stress time for the same devices. All of these transistors are from the same wafer and were processed identically except for the manner in which they were sintered. Wafers sintered in deuterium exhibit much more resilience to channel hot carrier stress. In our comparative study, we have electrically stressed 80 or so transistors, and have observed the same strong trend. These results have also been verified by performing the same electrical stress experiments on a second wafer from another lot. If we use 20% g_m degradation as a lifetime criterion, transistors sintered in deuterium typically have lifetimes 10–50 times longer than those sintered in hydrogen. Likewise, we observe a factor of 10 improvement in lifetime if we take a shift of 200 mV in threshold voltage as the degradation criterion. In our opinion,

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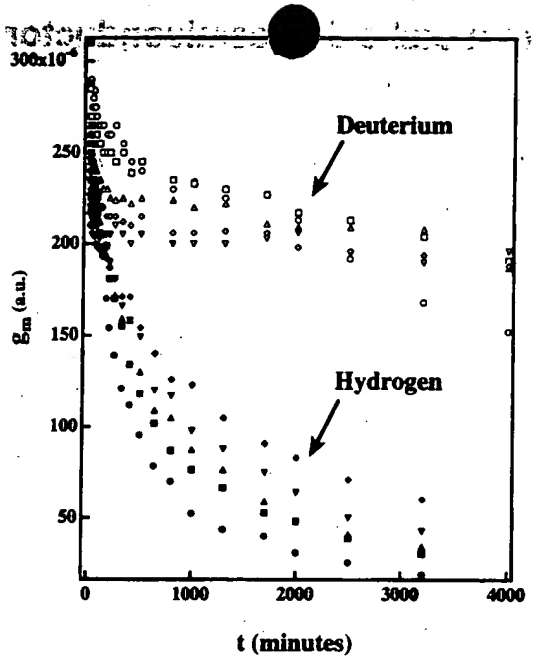

FIG. 1. Comparative time-dependent degradation of the transconductance g_m for five NMOS transistors sintered in hydrogen (solid symbols) and deuterium (unshaded symbols). The sinter process was performed in a 90% N_2:10% $H_2(D_2)$ ambient at 400 °C for 1 h.

further improvements in lifetime will be achieved once the optimum sinter process conditions are determined.

The theoretical explanation of the reduced hot electron degradation due to deuterium treatment is probably analogous to the explanation for the STM experiments by Avouris *et al.*,[8] although this analogy should not be pushed too far. They showed that hydrogen absorbed on the silicon surface can be taken off by a STM tip up to 100 times easier than deuterium. An explanation of such a giant isotope effect can be found by assuming that the hot electrons cause a population of a silicon–hydrogen (deuterium) antibonding state. This results in a force that accelerates the hydrogen away from the silicon surface leading to reduced wave function overlap with bulk silicon states. That acceleration is, of course, much diminished for the deuterium because of its bigger mass. For the same reason the kinetic energy gain necessary for dissociation is reached faster by hydrogen than by deuterium. In other words, the differences between hydrogen and deuterium arise from dynamic effects as they are important in chemical reactions. The static chemical bonding is evidently the same for both hydrogen and deuterium which is the reason for the identical transistor properties after hydrogen and deuterium treatment before hot electron dynamics and resultant damage. The difference of the hot electron degradation compared to the STM experiment lies mainly in the more complex chemistry of the Si/SiO_2 interface. The hydrogen (deuterium) passivating a silicon bond may (due to hot electron excitation) transfer to the SiO_2, passivating a more removed silicon bond or linking up with oxygen or even forming H_2 (D_2). All of these processes may be complicated by processes of interface reconstruction and defect chemistry. As a consequence, the energy needed to depassivate and remove hydrogen (deuterium) may be significantly different from the energies in the STM experiments. The close proximity of SiO_2 (instead of the more remote tip) will also permit different reactions of hydrogen (deuterium) than the "reaction" with the tip electrode.

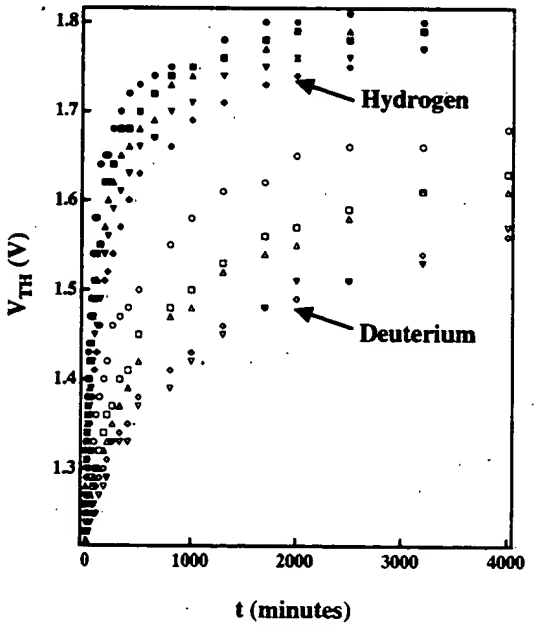

FIG. 2. Comparative time-dependent increase of the threshold voltage V_{th} for NMOS transistors sintered in hydrogen (solid symbols) and deuterium (unshaded symbols). These are the same five devices shown in Fig. 1.

In addition to the effects discussed above there are also other effects that may explain the large improvement of hot electron degradation by use of deuterium. One effect is the well-known isotope effect that relates to the larger zero point energy of the Si–H oscillations as compared to Si–D. Another effect is the possibility of excited Si–H or Si–D oscillations. Hot electrons in devices may excite by multiple impact oscillations far above the thermal equilibrium and thus force dissociation. A multiple excitation mechanism is also thought to explain hydrogen desorption at lower electron energies in the STM experiments.[9] Again, deuterium would show less energy transfer because of its large mass. Another explanation is related to the possible mass dependence of tunneling of the nuclei that might be involved in the chemical process of dissociation. We do not want to speculate at this point on which effect is dominant. All of these effects favor deuterium as the more stable passivation. The generality of these effects suggests that deuterium instead of hydrogen may be beneficial in other processes, devices, and device materials. Note that the well-known effects based on differing mobilities of H^+ and D^+ (e.g., following gamma irradiation[10]) or as occurring in electrolysis will not explain the giant isotope effect that we observe. These effects do not involve hot electrons at the interface.

In conclusion, we have demonstrated that the replacement of hydrogen with deuterium during the final wafer sintering process results in substantially reduced susceptibility to hot electron degradation effects. The explanation of the effect is based on the increased difficulty to break the deuterium bond due to the additional neutron mass.

This work was supported by the Office of Naval Research University Research Initiative under Grant N00014-92-J-1519 and by the Beckman Institute for Advanced Science and Technology at the University of Illinois. The use of the AT&T Silicon Fabrication Facility in Orlando (OR-1) is gratefully acknowledged. We also acknowledge many valuable discussions with Dr. Jiri Jonas. (J. L.) would like to thank Dr. Ph. Avouris, G. Abeln, and Dr. T.-C. Shen for valuable discussions and collaboration in the STM experiments. (K. H.) would like to thank Dr. P. von Allmen, Dr. T. L. Brown, Dr. G. J. Iafrate, Dr. E. H. Poindexter, and Dr. P. Wolynes for valuable discussions. (I.C.K.) thanks Dr. K.-H. Lee, Dr. G. Higashi, and Dr. D. P. Chesire for their encouragement.

[1] S. Wolf, *Silicon Processing for the VLSI Era* (Lattice, Sunset Beach, 1995), Vol. 3, Chap. 9, pp. 669–674.
[2] A. B. Fowler, U.S. Patent No. 3,849,204 (1974).
[3] J. W. Lyding, T.-C. Shen, J. S. Hubacek, J. R. Tucker, and G. C. Abeln, Appl. Phys. Lett. **64**, 2010 (1995).
[4] Ph. Avouris and J. W. Lyding (private communication).
[5] G. C. Abeln, T.-C. Shen, Ph. Avouris, and J. W. Lyding (unpublished).
[6] I. C. Kizilyalli, M. J. Thoma, and F. L. Lytle, IEEE Trans. Semicond. Manuf. **8**, 440 (1995).
[7] J. M. Pimbley, M. Ghezzo, H. G. Parks, and D. M. Brown, in *Advanced CMOS Process Technology* (Academic, San Diego, 1989), Vol. 19.
[8] Ph. Avouris, R. E. Walkup, A. R. Rossi, H. C. Akpati, P. Nordlander, T.-C. Shen, G. C. Abeln, and J. W. Lyding, Surf. Sci. (to be published).
[9] T.-C. Shen, C. Wang, G. C. Abeln, J. R. Tucker, J. W. Lyding, Ph. Avouris, and R. E. Walkup, Science **268**, 1590 (1995).
[10] N. S. Saks and R. W. Rendell, IEEE Trans. Nucl. Sci. **39**, 2220 (1992).

IEEE ELECTRON DEVICE LETTERS, VOL. 18, NO. 3, MARCH 1997

Deuterium Post-Metal Annealing of MOSFET's for Improved Hot Carrier Reliability

I. C. Kizilyalli, J. W. Lyding, and K. Hess

Abstract—**Low-temperature post-metallization anneals in hydrogen ambients are critical to CMOS fabrication technologies in reducing Si/SiO_2 interface trap charge densities by hydrogen passivation. In this letter we show that the hot carrier reliability (lifetime) of NMOS transistors can be increased by an order of magnitude when wafers are annealed in a deuterium ambient. This phenomenon can be understood as a kinetic isotope effect. The chemical reaction rates involving the heavier isotopes are reduced, and consequently, under hot electron stress, bonds to deuterium are more difficult to break than bonds to protium (H). However, the static chemical bonding (i.e., binding energies and excited states) is evidently the same for both hydrogen and deuterium. We measure identical transistor function after hydrogen and deuterium treatment before hot electron dynamics and resultant damage. Therefore, deuterium and hydrogen post-metal anneal processes are compatible with each other in semiconductor manufacturing. SIMS analysis proves that at typical anneal temperatures (400–450 °C), deuterium diffuses rapidly through the interlevel oxides and accumulates at Si/SiO_2 interfaces. Transistor speed versus reliability trade-off in CMOS device design is discussed in light of the findings of this study.**

I. Introduction

THE DEGRADATION of MOS transistor performance resulting from channel hot electrons has been an area of considerable study [1]. According to established theory, this aging process occurs as the result of hot electrons stimulating the desorption of hydrogen from the Si/SiO_2 (channel/gate-oxide) interface [2]. The process of post-metallization anneal of the wafers at low temperatures in hydrogen ambients improves device function by passivating the otherwise electrically active interface traps [3], [4], but it sets the stage for subsequent hot electron degradation. We have recently demonstrated an alternative process during which the interface states are passivated by deuterium instead of hydrogen [5], and have reported NMOS transistor lifetime improvements of larger than a factor of 10. The idea of using deuterium was inspired by experiments where a scanning tunneling microscope (STM) was used to stimulate the desorption of hydrogen or deuterium from Si(100)2 × 1:H(D) surfaces under ultrahigh vacuum conditions [6]–[10]. It was discovered that deuterium is much more difficult to remove under the conditions used to desorb hydrogen.

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In this letter, we provide recent measurements from a second lot experiment to show that deuterium and hydrogen post-metal anneal processes are compatible with each other for device function and use in semiconductor manufacturing. Speed versus reliability trade-off in CMOS device design is briefly discussed.

II. Experiments and Discussion

After the first level of metal processing [11], uncapped wafers and wafers capped with SiN were subjected to a deuterium sintering process. No improvement in transistor hot electron lifetimes was observed if the sinter step was performed after the wafers were capped with SiN. Clearly, SiN is a barrier for the diffusion of hydrogen as well as deuterium. Note that in this case, the passivation of the Si/SiO_2 interface still occurs via hydrogen that is present in large quantities in plasma deposited dielectric films [12]. Fig. 1 shows the secondary ion mass spectroscopy (SIMS) profile through the first interlevel oxide and silicon for two uncapped samples annealed in hydrogen and deuterium at 400 °C for 1 h. Deuterium is present in the interlevel oxide at concentrations of 10^{19} cm^{-3} and accumulates at Si/SiO_2 interfaces.

Transistors annealed in hydrogen or deuterium prior to hot electron stress can not be distinguished in any region of operation (Fig. 2). It appears that deuterium and hydrogen are equally effective in reducing the interface trap charge density. This is because the energies involved in chemical bonding are the same for both isotopes and consequently the equilibrium properties are the same.

Accelerated hot carrier dc stress experiments were performed on NMOS transistors at peak substrate current conditions. The interface damage, caused by hot carriers, is observed by monitoring the change in the linear transconductance (g_m) and threshold voltage (V_{th}) of the NMOS transistor. Fig. 3 shows the V_{th} degradation as a function of stress time. Fig. 4 shows NMOS transistor lifetime versus substrate current. Clearly, devices annealed in deuterium are much more robust under channel hot electron stress. The extrapolated transistor lifetimes are indicated using various degradation criteria. The large lifetime difference between the two anneal processes is apparent. It is noted that the substrate current specification for this technology can be increased by a factor of 2 while achieving equivalent hot electron degradation lifetime when deuterium is substituted for hydrogen in the post-metal anneal process.

Kinetic isotope effects connected to deuterium and hydrogen dissociation from surfaces have been extensively

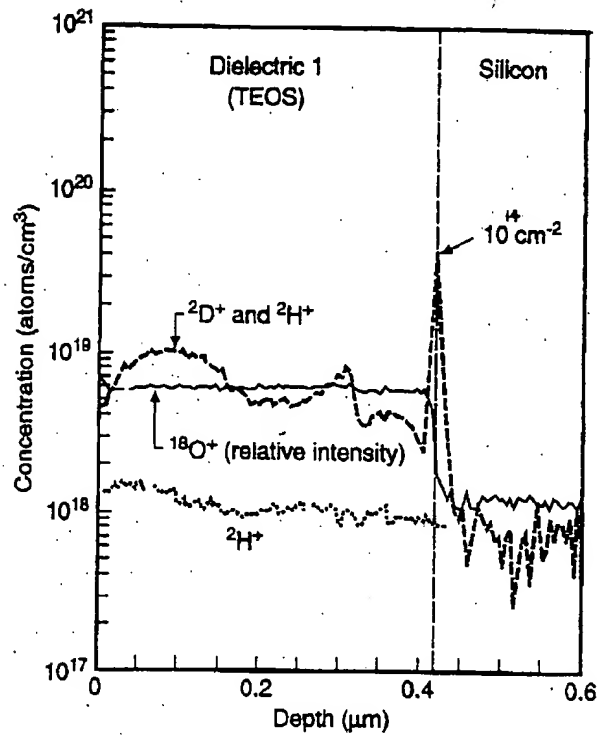

Fig. 1. SIMS profiles for deuterium, hydrogen, and oxygen. $^{18}O^+$ is monitored to locate the SiO_2/Si interface. The $^2D^+$ concentration can be inferred from the difference between the $^2H^+$ profiles for wafers annealed in deuterium and hydrogen (figure courtesy of F. Stevie) [13].

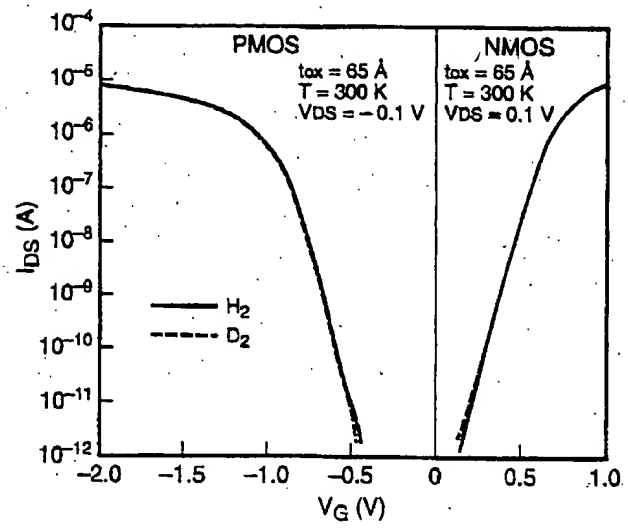

Fig. 2. Drain current versus gate voltage for NMOS and PMOS transistors annealed in forming gas with deuterium and hydrogen ambients. The anneal time is 1 h and performed at 400 °C.

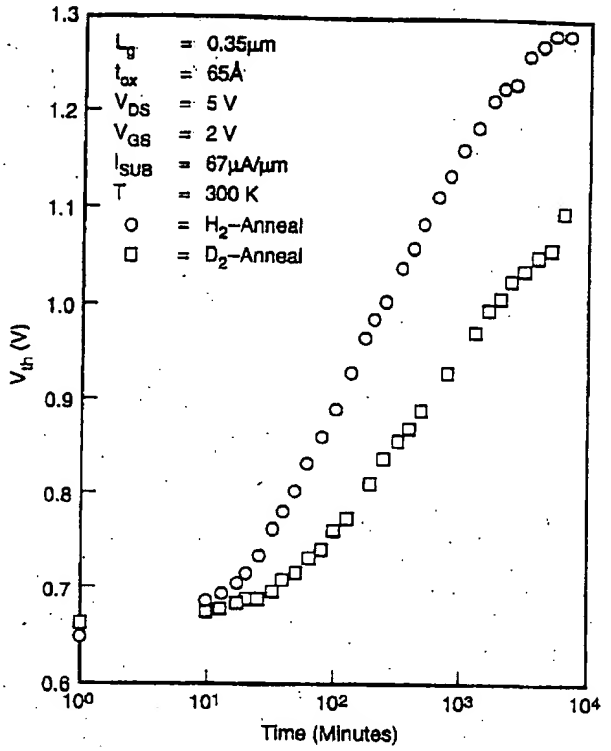

Fig. 3. Degradation of V_{th} versus time. The transistors were fabricated using a development version of Lucent's 0.35-μm CMOS technology where $L_G = 0.35$ μm, $I_{ON} = 600$ μA/μm, and $V_{th} \approx 0.65$ V. LDD regions are implanted with arsenic. The stressed transistors are from the same wafer and are processed identically except for the manner in which they are annealed.

reported in the literature in different context. We believe that the existence of a large isotope effect in hot electron degradation demonstrates that degradation occurs due to one of the well-known isotope mechanisms, for example the Mentzel–Gomer–Redhead effect [14]. There are other isotope sensitive mechanisms. However, they are very similar and we describe only one as a typical example. The hot electrons of the silicon conduction channel excite the electron of the silicon-hydrogen (deuterium) bond into an antibonding state. This results in a force accelerating the hydrogen away from the surface and leads to dissociation. Deuterium, because it is twice as heavy, does not accelerate as rapidly and the electron returns to the bonding state before dissociation occurs. This simplified description shows the principle: in the process of dissociation the mass of the atom plays a significant role (the exact model shows that it enters exponentially) and a large kinetic isotope effect is the consequence. We would like to point out that this model permits a complete physical description of hot electron damage from the energetic electron to the creation of the dangling bond. Such a model is then also able to distinguish the relative importance of single and multiple electron excitation. This should also give indication then whether the lowering of operating voltages can or can not eliminate damage completely. Obviously, if single excitation is the mechanism, the effect will be reduced as soon as the operating voltages are too small to cause excitation of an electron to the antibonding state. Multiple electron excitations would not permit such conclusions. Note also that the generality of the isotope effect gives a very strong indication that degradation which does not exhibit isotope differences is not related to simple hydrogen desorption. Isotope studies of all possible degradation mechanisms should provide important clues for their origin.

The impact of this study on the existing sub-0.5-μm CMOS technologies (3.3 and 5 V) is obvious, especially for those technologies where standard hot electron degradation criteria

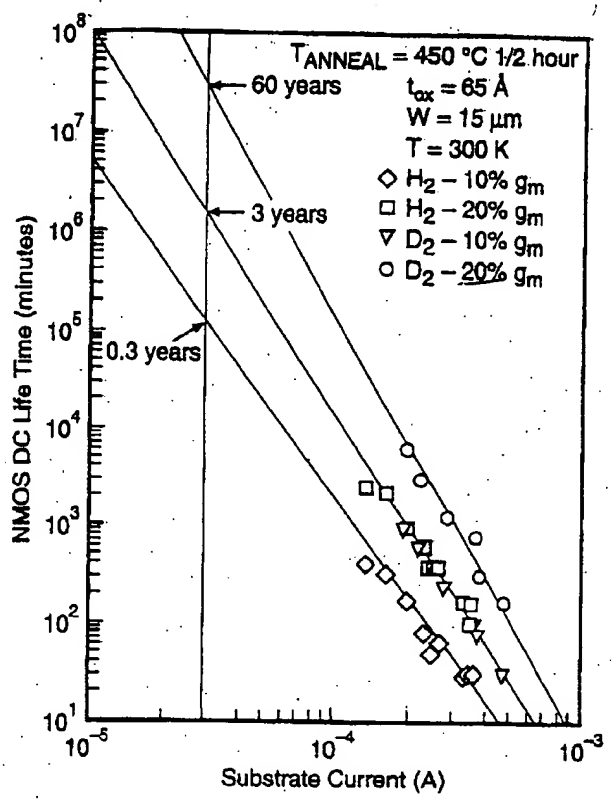

Fig. 4. Hot electron degradation lifetime versus substrate current. Stress voltages of $V_{DS} \approx 4.2$–4.6 V were used. A substrate current specification of $I_{SUB} = 2000$ nA/μm at $V_{DS} = 3.3$ V is assumed.

such as 10% g_m degradation in one year are barely met [15]. Possibilities of further feature size reduction and more aggressive drain engineering, with constant supply voltages, are offered by our technique. However, it is very difficult to be quantitative. This is because constraints imposed by hot electron effects are only one of the many other considerations that determine the minimum allowed gate length for a technology.

We have experimentally established that, for the deuterium anneal process to have the desired effect of enhancing the hot carrier reliability of a transistor, it must be performed prior to a SiN cap process. The questions, *whether a multilevel metallization or a SiN cap process renders the deuterium anneal ineffective*, have not been answered here and are topics of current research.

III. Conclusion

In this letter we have shown that the hot carrier reliability (lifetime) of NMOS transistors annealed in deuterium can be increased by an order of magnitude over those annealed in hydrogen. We interpret this phenomena as a kinetic isotope effect. Identical pre-degradation transistor properties after hydrogen and deuterium treatment are measured, suggesting that deuterium and hydrogen post-metal anneals are compatible processes for semiconductor manufacturing. SIMS analysis prove that deuterium diffuses rapidly through the interlevel oxides and accumulates at the Si/SiO_2 interface. Deuterium annealing may allow further transistor size reduction by relaxing the constraints imposed by hot electron effects.

Furthermore, we propose that the demonstrated isotope effect is relevant for improving the reliability of devices based on the hydrogenated (deuterated) amorphous-silicon material system (e.g., solar cells) where dangling bond defects are caused by exposure to light and fields.

Acknowledgment

The use of Lucent Technologies silicon fabrication facility in Orlando, FL, (OR-1) is gratefully acknowledged. The authors also acknowledge many valuable discussions with J. Jonas, P. von Allmen, T. Brown, G. Iafrate, E. Poindexter, P. Wolynes, Ph. Avouris, G. Abeln, T. Shen, D. Brady, J. Bude, D. Chesire, J. Clemens, R. Gregor, G. Higashi, S. Hillenius, J. Kearney, K.-H. Lee, P. K. Roy, R. Singh, M. Melliar-Smith, F. Stevie, R. Sun, and M. Thoma.

References

[1] J. M. Pimbley, M. Ghezzo, H. G. Parks, and D. M. Brown, *Advanced CMOS Process Technology, VLSI Electronics Microstructure Science*. San Diego, CA: Academic, 1989, vol. 19.
[2] R. C. Sun, J. T. Clemens, and J. T. Nelson, "Effects of silicon nitride encapsulation on MOS device stability," in *Proc. IEEE Int. Reliab. Phys. Symp.*, 1980, pp. 244–251.
[3] E. Cartier, J. H. Stathis, and D. A. Buchanan, "Passivation and depassivation of silicon dangling bonds at the Si/SiO_2 interface by atomic hydrogen," *Appl. Phys. Lett.*, vol. 63, pp. 1510–1512, 1994.
[4] A. B. Fowler, U.S. Patent 3 849 204, 1974.
[5] J. W. Lyding, K. Hess, and I. C. Kizilyalli, "Reduction of hot electron degradation in MOS transistors by deuterium processing," *Appl. Phys. Lett.*, vol. 68, pp. 2526–2528, 1996.
[6] J. W. Lyding, T.-C. Shen, J. S. Hubacek, J. R. Tucker, and G. C. Abeln, "Nanoscale patterning and oxidation of H-passivated Si(100)-2×1 surfaces with an ultrahigh vacuum scanning tunneling microscope," *Appl. Phys. Lett.*, vol. 64, pp. 2010–2012, 1995.
[7] Ph. Avouris and J. W. Lyding, private communication.
[8] G. C. Abeln, T.-C. Shen, Ph. Avouris, and J. W. Lyding, unpublished.
[9] T.-C. Shen, C. Wang, G. C. Abeln, J. R. Tucker, J. W. Lyding, Ph. Avouris, and R. E. Walkup, "Atomic-scale desorption through electronic and vibrational excitation mechanisms," *Science*, vol. 268, pp. 1590–1592, 1995.
[10] Ph. Avouris, R. E. Walkup, A. R. Rossi, H. C. Akpati, P. Norlander, T.-C. Shen, G. C. Abeln, and J. W. Lyding, "Breaking individual chemical bonds via STM-induced excitations," to be published.
[11] I. C. Kizilyalli, M. J. Thoma, S. A. Lytle, E. P. Martin, R. Singh, S. C. Vitkavage, P. F. Bechtold, J. W. Kearney, M. Ramband, M. Twiford, W. Cochran, L. Fenstermaker, R. Freyman, W. Sun, and A. Duncan, "High-performance 3.3- and 5-V 0.5-μm CMOS technology for ASIC's," *IEEE Trans. Semiconduct. Manufact.*, vol. 8, pp. 440–448, 1995; also in I. C. Kizilyalli, S. Lytle, B. R. Jones, E. Martin, S. Shive, A. Brooks, M. Thoma, R. Schanzer, J. Sniegowski, D. Wroge, R. Key, J. Kearney, and K. Stiles, "A very high-performance and manufacturable 3.3-V 0.35-μm CMOS technology for ASIC's," in *IEEE CICC Tech. Dig.*, 1996, pp. 31–34.
[12] A. C. Adams, "Dielectric and polysilicon film deposition," in *VLSI Technology*, S. M. Sze, Ed. New York: McGraw-Hill, 1983.
[13] F. A. Stevie, private communication.
[14] R. D. Ramsier and J. T. Yates, Jr., "Electron-stimulated desorption: Principles and applications," *Surf. Sci. Rep.*, vol. 12, pp. 243–378, 1991.
[15] See any one of many papers in *Proc. IEEE Int. Phys. Reliab. Symp.*, 1979–1995.

The Combined Effects of Deuterium Anneals and Deuterated Barrier-Nitride Processing on Hot-Electron Degradation in MOSFET's

Thomas G. Ference, Jay S. Burnham, William F. Clark, Terence B. Hook, Steven W. Mittl, Kimball M. Watson, and Liang-Kai Kevin Han

Abstract—**This paper describes the combined effects of deuterium anneals and deuterated barrier-nitride processing on hot-electron degradation in MOSFET's. Devices subjected to a 60-min, 400 °C, 10% deuterium/90% nitrogen anneal after silicidization show a 32× improvement in hot-electron lifetime. These same devices are then passivated with a deuterated barrier-nitride layer formed using deuterated ammonia (ND_3) and conventional silane (SiH_4). Further deuterium anneals along with conventional contact and metal-level processes are used to integrate the devices. Hot-electron stressing and SIMS analysis performed at various points in the processing give insight to methods of retaining the beneficial effects of deuterium during subsequent thermal processing.**

Index Terms—**Annealing, deuterium, hot carriers, MOSFET's, nitride, ND_3, semiconductor, SiD_4, surface states.**

I. Introduction

DESPITE aggressive scaling of the power supply voltage in leading-edge technologies, the integrity of gate oxide remains a key reliability issue. The field across the gate oxide has generally increased with scaling, and hot-electron shifts continue to plague the FET's, even at 1.5 nm [1]. Although electrons may readily tunnel out of the oxide when it is only 3.5-nm thick or less, damage to the silicon/silicon dioxide interface is not so easily avoided. From the viewpoint of device design, the electric field may be reduced by compromising device performance by adding a resistive lightly doped drain region. From the perspective of the process, various approaches to mitigating this damage have met with varying degrees of success. The addition of impurities such as fluorine and chlorine to the interface have a beneficial effect on the hot-electron and X-ray damage immunity [2]. Nitrogen, an additive to the oxide, has recently found widespread use [3], [4]. For nitrogen, improved hot-electron response is accompanied by other effects such as retardation of boron penetration and degradation of the electron mobility. Improvement of lifetime on the order of 2–5× is typical for nitrided oxides. It is invariably necessary to add hydrogen to the interface to reduce the number of as-oxidized interface traps and stabilize the threshold voltage, but super-saturation of the oxide with hydrogen during dielectric deposition dramatically degrades the NFET lifetime [5]. However, substituting deuterium for hydrogen at the standard interface passivation anneal step improves the NFET lifetime by a factor of 10–100 [6]–[8]. The exact mechanism of this improvement is not known, but is believed to be related to the mass of the passivating species because the chemistry of the two species is nearly identical [7]. When the passivating species at the silicon/silicon-dioxide interface is deuterium instead of hydrogen, there is no doubt that the interface is more robust to hot-electron damage [6]–[8]. The technological difficulty is in placing and retaining the deuterium at the interface in a hydrogen-rich environment. During device fabrication various key films such as silane, ammonia, TEOS, and forming gas are formed from hydrogenated gases. Even the very last process steps can affect the hydrogen concentration in the gate oxide [5], [9].

This work investigates a novel method for incorporating deuterium into MOSFET devices. Past efforts have focused on diffusing deuterium into the gate region of devices with an anneal in a deuterium ambient [6]–[9]; the anneals were performed after a device was fabricated (after the first level of metallization). Annealing at this step in the processing has the drawback of requiring deuterium to diffuse through multiple layers as well as having to be compatible with typical back-end-of-line (BEOL) processing. To have minimal impact on metal sheet resistance, a low-temperature anneal is required. The lower the anneal temperature, the less effective it is to diffuse deuterium to the gate region. We propose to incorporate deuterium directly into the device by using a deuterated precursor species to fabricate a deuterated silicon-nitride reservoir and a barrier to subsequent in-diffusion of hydrogen and out-diffusion of deuterium. This approach makes the deuterium-enrichment process independent of BEOL processing. As part of this overall investigation, variations in the device structure and the anneals have also been evaluated to gain insight to methods of retaining the positive deuterium effects.

II. Experimental Procedure

A. Device Structure

A 0.35-μm, 5-nm gate oxide, 2.5-V CMOS device was used to evaluate the effects of deuterium anneals and deuterated silicon-nitride processing on hot-electron degradation; 200-

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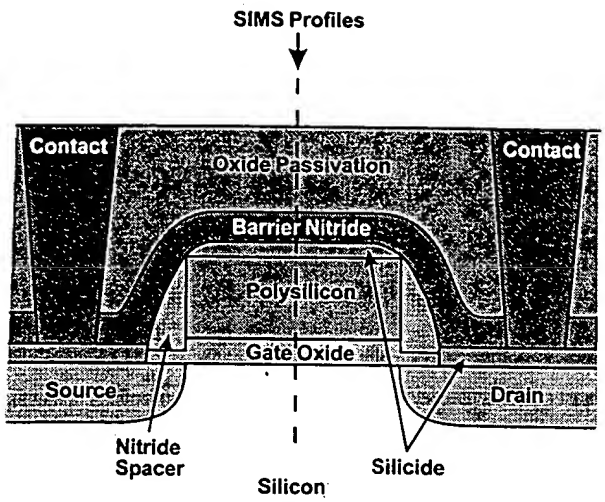

Fig. 1. CMOS device structure used in experiments.

mm wafers with fully integrated devices were used in all the experiments. The basic structure of the device is shown in Fig. 1. Nitride spacers and the deuterated barrier-nitride layer are key features of this device that make it different from devices used by previous researchers [6]–[8] studying the effects of deuterium on device lifetime. The barrier-nitride layer is used both as an etch stop for the contact etch and as a barrier to ionics from BEOL dielectrics and metallurgy.

B. Anneals

All anneals were carried out in a vertical anneal furnace using a forming gas ambient. For the deuterium anneals, the gas ambient was a mixture of 10% deuterium and 90% nitrogen. The hydrogen anneals used 10% hydrogen and 90% nitrogen. Different temperature and time conditions were used for the various anneals. Post-silicide and at first-metal anneals had a 400 °C, 60-min dwell. Post-liner deposition anneals had a 550 °C, 30-min dwell.

C. Nitride Formation

Formation of the silicon nitride was carried out using PECVD. For forming deuterated silicon nitride, ND_3 replaces NH_3, which provides the deuterium source.

D. Nitride Characterization

Rutherford backscattering spectrometry (RBS) methods were used to characterize the silicon-nitride films. The RBS instrumentation consisted of an NEC 5SDH accelerator with a Charles Evans and Associates RBS400 end station. A sample consisting of a blanket film on a silicon wafer was irradiated with 2.9 meV doubly charged helium (He^{2+}) ions in both standard and hydrogen forward-scattering geometries. The data was analyzed with the Rutherford Universal Manipulation Program (RUMP) and standardized with tungsten silicide. Table I indicates the RBS-derived compositions of the silicon-nitride films used in the fabrication of the devices evaluated in this paper. As stated previously, conventional silicon-nitride films were formed from SiH_4:NH_3, while deuterated films were formed with SiH_4:ND_3. The Si and N concentrations were the same for both types of films. The total concentration of hydrogen plus deuterium was 20 atomic percent for both films, with 45% being deuterium in the partially deuterated film.

TABLE I
RUTHERFORD BACKSCATTERING SPECTROMETRY MEASUREMENTS OF ELEMENTAL CONCENTRATION FOR PECVD NITRIDE DEPOSITED WITH (SiH_4 : NH_3) AND (SiH_4 : ND_3).

Formation Gases	Si	N	H	D	D/(H+D)
(SiH_4 : NH_3)	0.30	0.50	0.20	0.00	0%
(SiH_4 : ND_3)	0.30	0.50	0.11	0.09	45%

E. SIMS Analysis

Secondary ion mass spectrometry (SIMS) was utilized for film characterization of the integrated devices. The dashed line in Fig. 1 delineates where SIMS profiles were taken through a device to determine elemental compositions. A 150 μm×300 μm MOS capacitor with the same general structure illustrated in Fig. 1 was analyzed. The SIMS analyses were performed with Cameca IMS6f and IMS4f instruments. A 14.5-keV positive cesium (Cs^+) ion-beam sputtered the negative secondary hydrogen ($1H^-$) and deuterium ($2H^-$) ions that were detected after accelerating to 4.5 keV. Samples with insulating overlayers were either stripped in concentrated HF or gold-coated and analyzed with an electron flood for charge compensation. All analyses were calibrated with 1H and 2H implants in silicon. No attempt was made to correct for sensitivity differences in the oxide and nitride layers.

F. Device Lifetime Stress

Hot-electron lifetime was determined from stresses at four different V_{ds} (drain-to-source voltage) values with V_{gs} (gate-to-source voltage) chosen for peak substrate current at each V_{ds}. Reverse saturated I_{ds} (drain to source current) was used as the degradation parameter and was measured at $V_{ds} = 2.5$ V and $V_{gs} = 2.5$ V, with the source and drain interchanged from stress configuration. Stress voltages were applied until the reverse saturated I_{ds} was decreased by 10% or 30 000 seconds elapsed. The lifetime-to-10% decrease in reverse I_{ds} was interpolated or extrapolated from the data. Substrate current was measured at the beginning of the stress for each device.

III. EXPERIMENTAL RESULTS

The lifetime of devices fabricated with conventional hydrogen-containing materials and annealed in deuterium and hydrogen, post silicide, is plotted in Fig. 2. The devices were tested after anneal, but before further processing. The deuterium-annealed devices showed a 32× improvement over those annealed in hydrogen. Similar devices were then processed with conventional hydrogen-containing materials up to first-metal, where they were retested; the results are plotted in Fig. 3. These devices showed no difference between those annealed in hydrogen. It is surmised that the thermal processing subsequent to the deuterium anneal diluted the deuterium in the gate-oxide/silicon region with hydrogen to

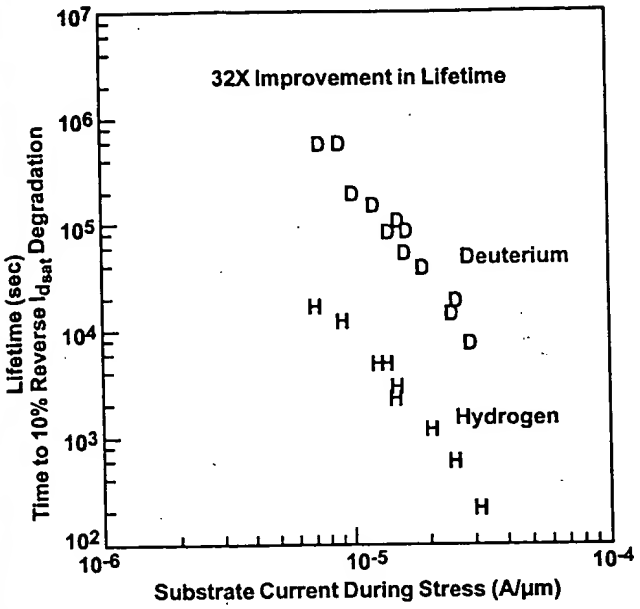

Fig. 2. NFET lifetime versus substrate current for 10% deuterium/90% nitrogen, 400 °C, 60-min anneal post silicide.

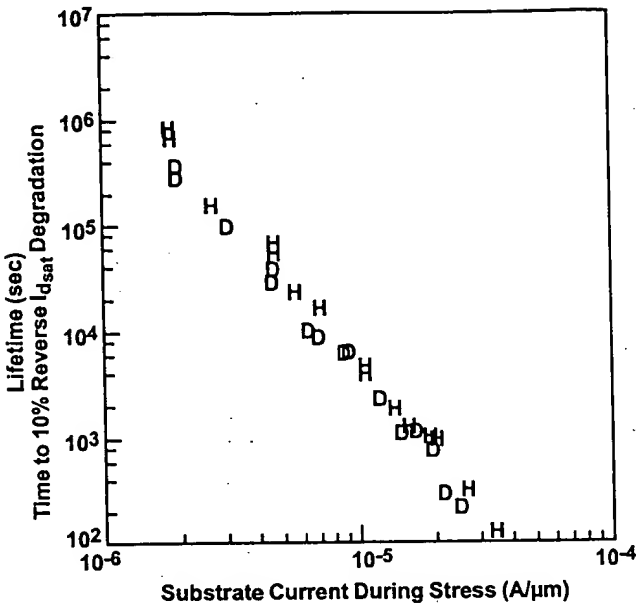

Fig. 3. NFET lifetime versus substrate current for 10% deuterium/90% nitrogen, 400 °C, 60-min anneal post silicide processed to first level of metal.

the point where the deuterium/hydrogen ratio was no longer high enough to reduce hot-electron degradation.

To obtain a better understanding of how deuterium anneals affect deuterium concentrations in the gate region of a device, deuterium anneals were done on two device structures and at two different processing steps. Both devices were NFET's based on the structure in Fig. 1. One device had a barrier-nitride layer and the other was fabricated without the barrier-nitride layer. In both cases, all films were formed using conventional hydrogen-containing species. Deuterium anneals were done post-silicide and at the first-metal level. Anneal conditions were as described earlier in the experimental procedure. Fig. 4 shows SIMS profiles of the deuterium concentration in each device traversing through the silicide, polysilicon, the gate oxide, and into the silicon of the device gate region.

The devices annealed post-silicide and, corresponding to the 32× improvement discussed earlier, showed significant amounts of deuterium in the polysilicon gate, with more in the gate-oxide region. The device without nitride and annealed at first-metal had substantially less deuterium integrated into the device. The device with the nitride layer and annealed at first-metal had almost no deuterium incorporated into the device. These results reveal that the nitride layer acts as a barrier to deuterium diffusion during the anneal at first-metal and that, without the nitride layer, deuterium can diffuse into the gate-oxide region even if the device has nitride spacers.

To further understand the role that the nitride layer plays, SIMS profiles were taken through a sample containing a nitride layer, silicide, polysilicon, gate oxide, and silicon of a device that was annealed at silicide with deuterium and had the partially deuterated silicon-nitride film described earlier. With the blanket barrier nitride in place, the lifetime improvement could not be tested for the devices at this point. This composition profile, shown in Fig. 5, reveals that the nitride film contains three orders of magnitude more

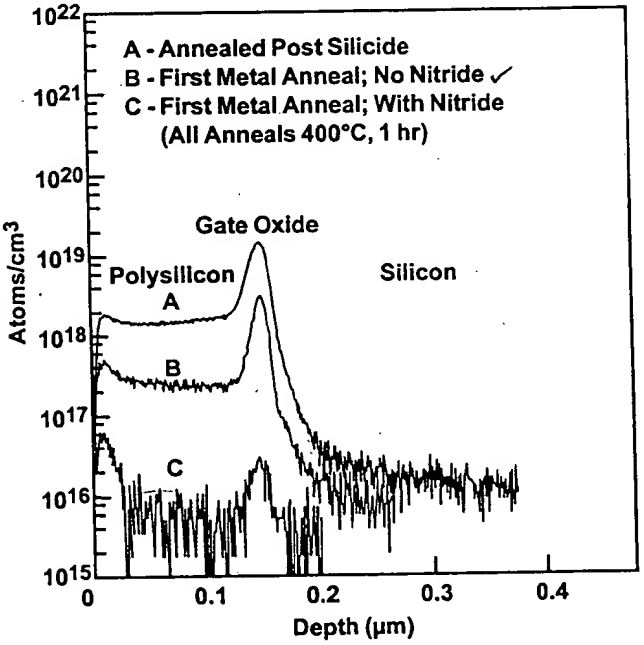

Fig. 4. SIMS deuterium profiles for anneals of different structures.

deuterium/hydrogen than the gate-oxide region of the device. The nitride film acts as a reservoir for deuterium/hydrogen. This easily explains how the 32× improvement seen in the sample annealed in deuterium post silicide was diluted when the hydrogen-containing nitride layer was deposited and put through other BEOL thermal processing. The silicide and polysilicon provide a diffusion path between the H reservoir in the nitride and the gate oxide. We also observed the following from the composition profile in Fig. 5.

1) The higher concentration of hydrogen indicated in the polysilicon and silicon is an artifact of the background level in the SIMS tool.

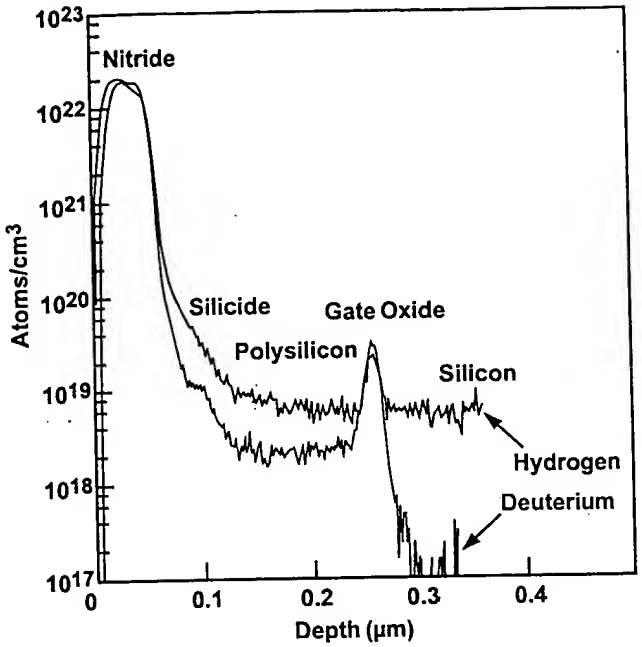

Fig. 5. SIMS profiles of the gate-structure composition with deuterated nitride.

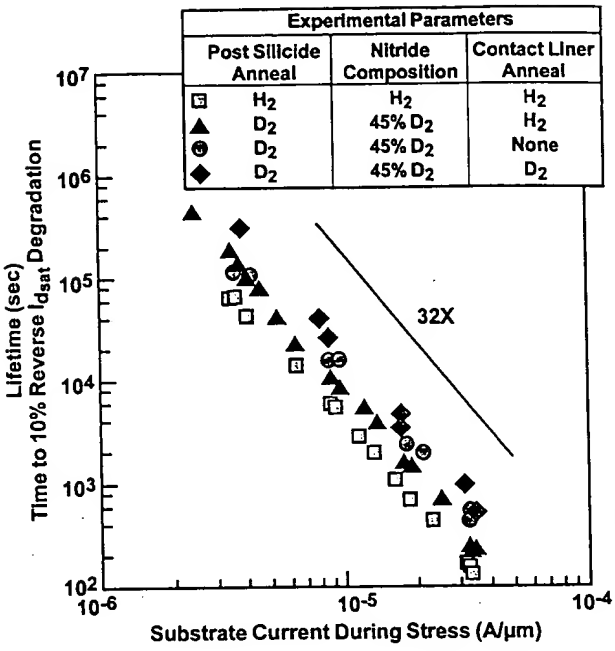

Fig. 6. NFET lifetime versus substrate current post contacts for various experimental parameters from silicide to contacts.

2) The deuterium preferentially segregates to the gate-oxide/silicon region of the device. The use of an implant in silicon to calibrate the profiles actually leads to erroneous concentrations of deuterium and hydrogen in the gate-oxide region.
3) The nitride film contains almost equal amounts of deuterium and hydrogen and correlates well with the RBS data shown in Table I.

Given that the silicon-nitride film used in these devices acts both as a barrier to hydrogen and to deuterium diffusion across it and as a reservoir for deuterium and hydrogen, an attempt was made to use the partially deuterated silicon-nitride film to retain deuterium's positive lifetime effect. Fig. 6 shows lifetime versus substrate current for devices fabricated with different process conditions at post-silicide surface anneal, nitride film composition, and contact liner anneal. Hydrogen-containing or deuterium-containing species were used at these process steps. All lifetime measurements were made after the formation of tungsten contacts. The results indicate that a post-silicide anneal to replace hydrogen at the gate-oxide/silicon interface, combined with the deuterated nitride reservoir, provides some improvement in device lifetime. This improvement can be further increased by combining it with no anneal or, better yet, a deuterium anneal at the contact-liner formation. This improvement in lifetime (~6×) with the contact liner anneal in deuterium is attributed to the fact that openings in the barrier-nitride layer allow a pathway for deuterium and hydrogen to pass through to the gate-oxide region of the device.

With a post-silicide deuterium anneal, deuterated silicon nitride, and deuterium contact-liner anneal, further processing to first-metal with conventional hydrogen-containing species shows that the device lifetime improvement at first-metal is exactly the same as that seen at contact level (Fig. 7). These

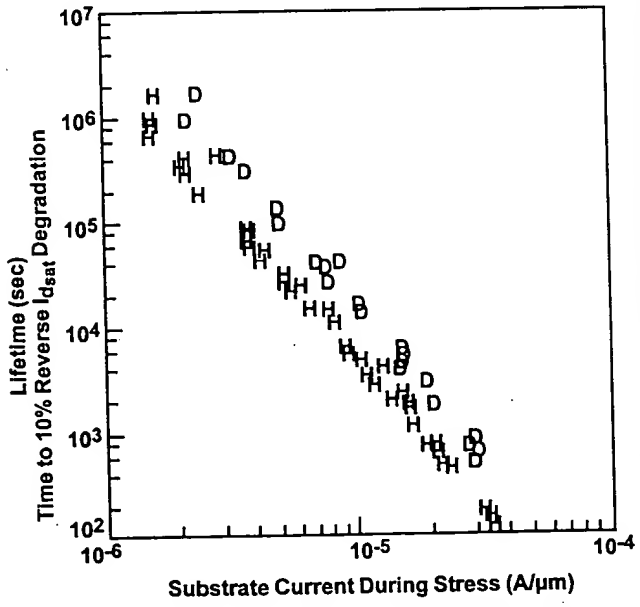

Fig. 7. NFET lifetime versus substrate current post first level of metal.

observations support the theory that, once the deuterium is incorporated into the device, equilibrated with a reservoir, and sealed with a diffusion barrier, further changes in the deuterium profile in the device are essentially independent of BEOL processing.

Although the partially deuterated silicon-nitride film can act as a deuterium reservoir and barrier to subsequent hydrogen processing, it never reached the 32× improvement seen after the silicide anneal in deuterium. Evaluating the device lifetime as a function of the percentage of deuterium at the gate-oxide/silicon-interface region allows us to better understand

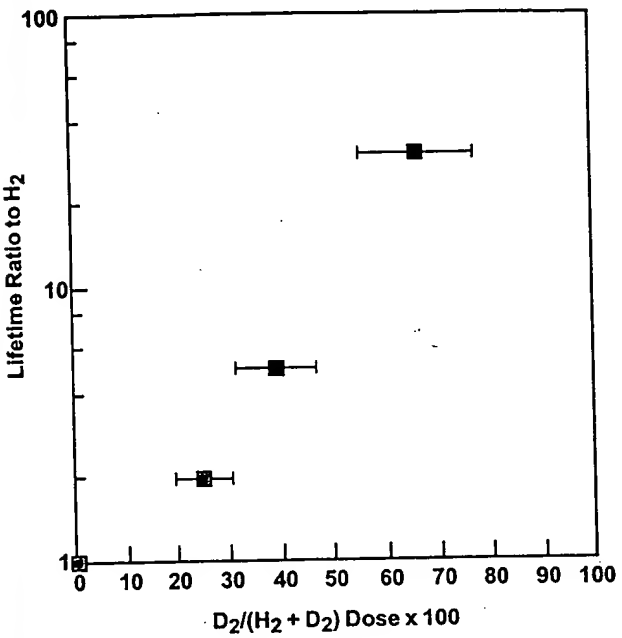

Fig. 8. Device lifetime versus percent deuterium in the gate-oxide/silicon interface region. (Error bars reflect the uncertainty in the precision of the SIMS measurements.)

the above results. Fig. 8 indicates the lifetime improvement as a function of deuterium concentration in the gate-oxide region. The deuterium percentage was calculated as a ratio of deuterium to the total amount of deuterium + hydrogen using SIMS dose data. This plot was generated from the SIMS data for the devices evaluated in this paper. For a device equilibrated with a reservoir containing 45% deuterium, one would expect a similar equilibrium composition of 45% deuterium in the gate-oxide/silicon region. For this deuterium concentration, the lifetime improvement predicted from the data in Fig. 8 would be 6×. Lifetime improvements of 10× or more can be expected only when more than 50% of the hydrogen in the gate-oxide/silicon region is replaced with deuterium. The graph also suggests that greater than 100× lifetime improvement is achievable if all the hydrogen is replaced by deuterium. This correlates well with the results of other researchers [8] who have seen up to a 100× improvement in lifetime using deuterium anneals.

IV. Deuterium Reservoir and Barrier Technique

The concept of a deuterium reservoir and barrier [10] lends itself to some unique processing and deuterium retention capabilities. With a deuterium reservoir and barrier, the number of processing steps that require deuterated materials can be limited and the BEOL processing can be independent of the front-end-of-line (FEOL) deuterium incorporation. This should ultimately reduce costs and give more flexibility in BEOL processing. The main purpose of the reservoir is to supply deuterium to the gate-oxide/silicon region, and the barrier's main purpose is to stop deuterium from leaving the gate-oxide/silicon region and to prevent hydrogen with subsequent processing from getting into the gate-oxide/silicon region that would dilute the deuterium already present. The barrier and reservoir can be separate films with their respective roles and properties or they can be a single film as used in the present study with the barrier-nitride layer.

Conceptually, the ideal process is to use conventional semiconductor processing up to a point; we selected post-silicide processing as our point. At that interval, as much hydrogen as possible should be replaced with deuterium in the device region. This is accomplished with the post silicide anneal. An alternative method is a vacuum anneal followed by a deuterium anneal as practiced by Autran *et al.* [11]. A large deuterium reservoir film is then used to cover the device. A reservoir can be any material containing high concentrations of deuterium and in close proximity to the gate-oxide/silicon region. This reservoir dilutes any residual hydrogen remaining in the device. A deuterium/hydrogen diffusion barrier layer is then added to prevent intermixing of deuterium and hydrogen from subsequent processing. (This allows BEOL processing to be done using conventional hydrogen-containing materials.) When making contacts to the devices, holes need to be opened through the reservoir and barrier layers; in this case, thermal processing should be done in a deuterium ambient until the openings are once again plugged with a "barrier" type material such as tungsten studs.

V. Conclusion

Up to a 32× improvement in device lifetime has been observed in CMOS devices annealed in a 10% deuterium/90% nitrogen ambient. The greatest improvement was seen after silicide anneal, with subsequent thermal processing degrading the effect. A device without silicon nitride and with a 10% deuterium/90% nitrogen anneal after first-metal showed less deuterium. A silicon-nitride layer incorporated on top of the device after silicide acted as a barrier to deuterium diffusion out of the gate-oxide/silicon region, and as a barrier to hydrogen diffusion into the gate-oxide/silicon region for anneals performed at first-metal.

Creating a deuterium reservoir/barrier in the form of a silicon-nitride layer on top of the device can improve deuterium retention during subsequent BEOL processing. For the experiments presented in this paper, the silicon-nitride layer is formed from a mixture of deuterated ammonia (ND_3) and conventional silane (SiH_4). The nitride layer incorporates a total of 20% hydrogen/deuterium with a ratio of deuterium to hydrogen of 0.45.

The ratio of deuterium to hydrogen at the gate-oxide/silicon region is key to determining the expected device lifetime improvement. SIMS data indicates that the improvement in lifetime is related exponentially to the ratio of deuterium to hydrogen, with lifetime improvements of up to 100× predicted for a fully deuterated gate-oxide/silicon region.

The combination of deuterium anneals and a fully deuterated nitride reservoir/barrier layer could be a viable method for retaining the positive effects of deuterium, making it possible to achieve a full 100× improvement in device lifetime. This improvement may be achieved in a way that is less sensitive to subsequent BEOL processing.

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REFERENCES

[1] H. Momose, S. Nakamura, T. Ohguro, T. Yoshitomi, E. Morifuji, T. Movimoto, Y. Katsumat, and H. Iuai, "A study of hot-carrier degradation in N- and P-MOSFET's with ultrathin gate oxides in the direct-tunneling regime," in *IEDM Tech. Dig.*, 1997, p. 453.

[2] I. Vishnubhotla, A. Balasinski, X. W. Wang, T. P. Ma, H. H. Tseng, and P. Tobin, "Mobility and reliability improvements of fluorinated gate oxide for VLSI technology," in *VLSI Symp.*, 1995, pp. 44–48.

[3] T. Hook, K. Watson, E. Lee, D. Martin, R. Ganesh, S. Kim, and A. Ray, "Correlation between fixed positive charge and hot-electron immunity for nitrided oxides," *Electron Device Lett.*, vol. 18, pp. 471–473, Oct. 1997.

[4] T. Hook, J. Piccirillo, K. Watson, and E. Nowak, "A CMOS technology for sub-5-nm, 3.3-V LVTTL 1 Mbit SRAM," in *Proc. ESSDERC*, 1995, pp. 531–534.

[5] J. Cheek, H. E. Nariman, D. Wristers, D. Nayak, and M. Y. Hoa, "Effect of local interconnect etch stop layer on channel hot electron degradation," in *Proc. SPIE Int. Soc. Opt. Eng.*, vol. 3212, pp. 268–274, 1997.

[6] J. W. Lyding, K. Hess, and I. Kizilyalli, "Reduction of hot electron degradation in metal oxide semiconductor transistors by deuterium processing," *Appl. Phys. Lett.*, vol. 68, no. 18, pp. 2526–2528, 1996.

[7] K. Hess, I. Kiziyalli, and J. Lyding, "Giant isotope effect in hot electron degradation of metal oxide semiconductor transistors," *IEEE Trans. Electron Devices*, vol. 45, pp. 406–416, Feb. 1998.

[8] I. C. Kizilyalli, Z. Chen, J. Lee, J. W. Lyding, and K. Hess, "Improvement of hot carrier reliability with deuterium anneals in manufacturing muti-level metal/dielectric MOS systems," *Electron Device Lett.*, vol. 19, pp. 444–446, Nov. 1998.

[9] W. F. Clark, T. G. Ference, T. B. Hook, K. M. Watson, S. W. Mittl, and J. S. Burnham, "Process stability of deuterium-annealed MOSFET's," *Electron Device Lett.*, vol. 20, pp. 48–50, Jan. 1999.

[10] W. F. Clark, T. G. Ference, T. B. Hook, and D. Martin, "Use of deuterated materials in semiconductor processing," U.S. patent pending.

[11] J. L. Autran, R. A. B. Devine, W. L. Warren, and K. Vanheusden, "Comparative hot carrier induced degradation in 0.25-μm MOSFET's with H or D passivated interfaces," in *Proc. ESSTERC*, Stutgart, Germany, Sept. 1997, pp. 580–583.

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